M3x5x Series
3.2x5.0 mm, SMT VCXO

FEATURES

Frequencies from 15 MHz to 2100 MHz
Low jitter: Typ. 130fs rms @622.08MHz
RF Output: CMOS, LVPECL, LVDS, CML or HCSL
Operating temperature range up to -40°C to +85°C
Operating Voltage: 1.8/2.5/3.3 V

APPLICATIONS

Test and Measurement
Industrial Controls
Optical Transmission

ORDERING INFORMATION

M3	x	5x	2	4	A	T	L	N	00.0000 MHz

Number of frequencies
0: Single
2: 2 Frequencies
4: 4 Frequencies

Supply Voltage
50: 3.3V **51:** 2.5V **52:** 1.8V

Temperature Range
1: 0°C to +70°C **2:** -40°C to +85°C
6: -20°C to +70°C

Stability
E: ± 10 ppm **8:** ± 20 ppm **4:** ± 50 ppm

Output Type
G: Enable High (pad 2) **M:** Enable Low (pad 2)
U: No Enable

Pull Range
1: ± 50 ppm **2:** ± 100 ppm **3:** ± 200 ppm

Symmetry/Output Logic
C: 45/55% CMOS **H:** 45/55% HCSL **L:** 45/55% LVDS
M: 45/55% CML **P:** 45/55% LVPECL

Package
N: Leadless SMT

Frequency (customer specified)

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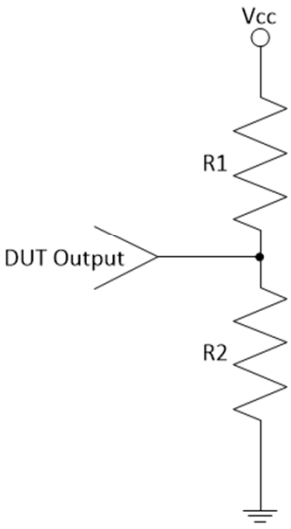
ELECTRICAL SPECIFICATIONS

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Frequency Range	F_0	15 15		2100 200	MHz MHz	CML, HCSL, LVPECL, LVDS CMOS
Frequency Stabilities						
vs. Operating Temperature	$\Delta F/F$	See ordering information			ppm	
RF Output						
Output Load		50Ω to (V_{CC} - 2) VDC 100Ω Differential 50Ω(V_{CC}) 50Ω 15pF				LVPECL LVDS CML HCSL CMOS
Frequency Adjustment						
Control Voltage Range	Vc	0.18 0.25 0.30	0.90 1.25 1.65	1.62 2.25 3.00	V V V	@ 1.8 V supply @ 2.5 V supply @ 3.3 V supply
Tuning Range		See ordering information			ppm	
Frequency Change Polarity		Positive or Negative				
Enable/Disable						
Enable/Disable Logic (Option G)		Input Logic “1” or floating Input Logic”0”				Output Enabled Output disabled to HIGH Z
Enable/Disable Logic (Option M)		Input Logic “0” or floating Input Logic”1”				Output Enabled Output disabled to HIGH Z
Temperature						
Operating Temperature	T_A	See ordering information				
Storage Temperature	T_S	-55		+125	°C	
Operating Voltage and Current						
Operating Voltage		2.970	3.300	3.630	V	Option 50
		2.375	2.500	2.625	V	Option 51
		1.710	1.800	1.890	V	Option 52
Operating Current				95	mA	LVPECL
				100	mA	HCSL
				85	mA	CMOS, LVDS
				80	mA	CML
Other Parameters						
Phase Jitter (RMS)	Φ_J		130		fs	12 KHz to 20 MHz 622.08MHz

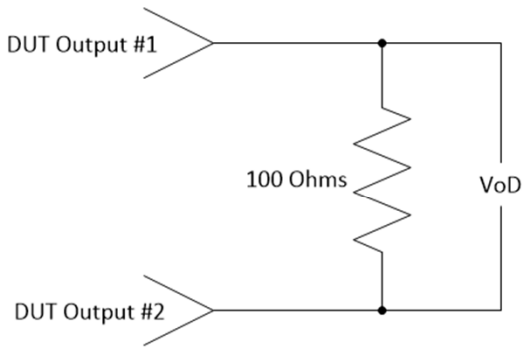
LOAD CIRCUIT DIAGRAMS

LVPECL Load Circuit

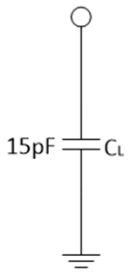


Vcc	R1 (Ohm)	R2 (Ohm)
3.3 V	124	82
2.5 V	250	62

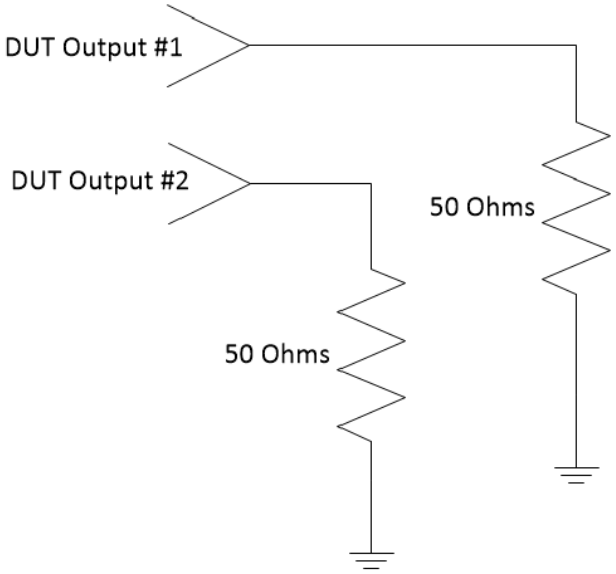
LVDS/CML Load Circuit



CMOS Load Circuit



HCSL Load Circuit



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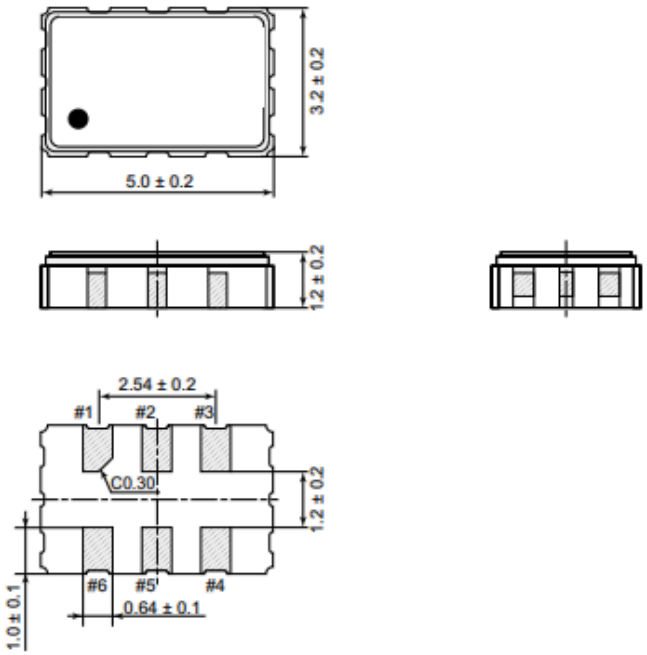
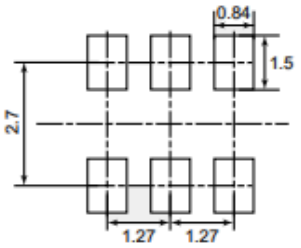
MECHANICAL AND PIN OUT INFORMATION – Single and Dual Frequency



SUGGESTED SOLDER PAD LAYOUT



Single Frequency	
Pad	**Function**
1	Voltage Control
2	Enable/Disable or N/C
3	Ground
4	Output Q
5	Output $\bar{Q}$ (N/C for CMOS)
6	Supply V_{DD}+

Dual Frequency	
Pad	**Function**
1	Voltage Control
2	Frequency Select 0
3	Ground
4	Output Q
5	Output $\bar{Q}$ (N/C for CMOS)
6	Supply V_{DD}+

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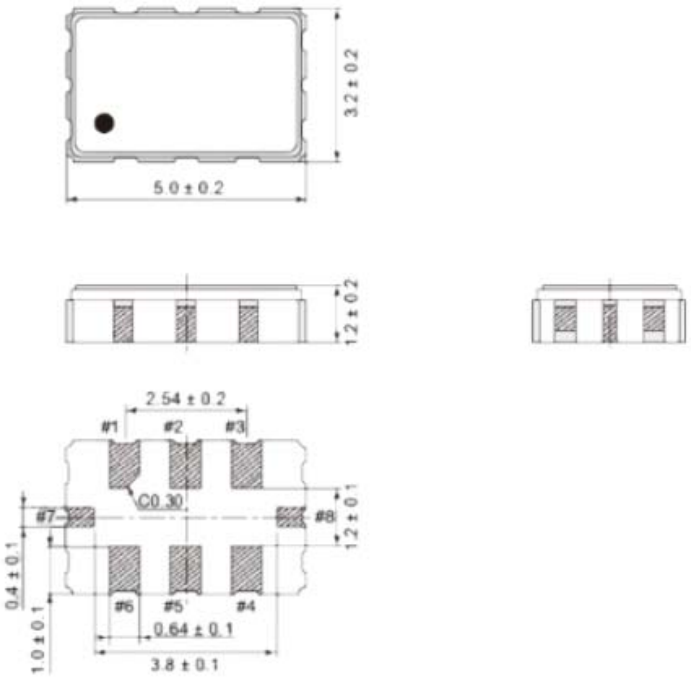
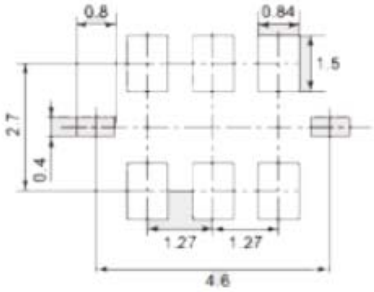
MECHANICAL AND PIN OUT INFORMATION – Four Frequencies



SUGGESTED SOLDER PAD LAYOUT



4 Frequencies	
Pad	**Function**
1	Voltage Control
2	Enable/Disable or N/C
3	Ground
4	Output Q
5	Output $\bar{Q}$
6	Supply Vcc+
7	Frequency Select 1
8	Frequency Select 0